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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/853,333	05/10/2001	Safi Khan	990407	7362

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Qualcomm Incorporated
Patents Department
5775 Morehouse Drive
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EXAMINER	
VO, TIM T	

ART UNIT	PAPER NUMBER
2189	6

DATE MAILED: 11/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)
	09/853,333	KHAN ET AL.
	Examiner	Art Unit
	Tim T. Vo	2189

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,15-23,32-41 and 48-53* is/are rejected.

7)☒ Claim(s) *7-14,24-31 and 42-47* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

Part III DETAILED ACTION

Notice to Applicant(s)

This application has been examined. Claims 1-53 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:
A person shall be entitled to a patent unless --

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claim 1-6, 21-23 and 39-41 are rejected under 35 U.S.C. § **102**(**b**) as being anticipated by Jayakumar et al. patent number 6,021,458 referred hereinafter "Jayakumar".

As for claims 1, 21 and 39, Jayakumar teaches a system for use in a mobile communication device, the system comprising:

A microprocessor having components for responding to interrupt requests by interrupt current processing and performing an interrupt service routine associated with the interrupt request (see figure 1, interrupts 110, interrupt controller comprising Acceptance Logic 112, Prioritizer 118, CPU Core 122 and column 4 line 60 to column 5 line 11, wherein the interrupts 110 come from different sources, the interrupt controller comprising acceptance logic 112 and prioritizer 118, they receives interrupts 110 and process the interrupt by determining interrupt request and their priority then send to the

CPU core 122). Peripheral processing units having components for generating interrupt requests for sending to the microprocessor (see figure 1, interrupts 110 and column 4 lines 63-66). an interrupt controller having components for receiving interrupt requests directed to the microprocessor from the peripheral processing units and for prioritizing the interrupt requests on behalf of the microprocessor (see figure 1, interrupt controller comprising acceptance logic 112, prioritizer 118 and column 4 lines 60 to column 5 line 11).

As for claims 2, 22 and 40, Jayakumar teaches wherein the interrupt controller includes:

an interrupt source interface unit for receiving interrupt requests directed to the microprocessor from the peripheral processing units (see figure 1interrupts 110, acceptance logic 112);

an interrupt prioritization unit for identifying an interrupt request of highest priority from among the interrupt requests received (see figures 1-2, prioritizer 118, HPI, HIS, vector and column 6 lines 17-49, wherein the prioritizer determines which requests has the highest interrupt priority in the Interrupt Request Register (IRR) is encoded and supplied as the interrupt vector. Once the vector information is forwarded to the processor);

a microprocessor notification unit for notifying the microprocessor of the interrupt request of highest priority. (see figures 1-2, prioritizer 118, HPI, HIS, vector and column 6 lines 17-49, wherein the prioritizer determines which requests has the highest

interrupt priority in the Interrupt Request Register (IRR) is encoded and supplied as the interrupt vector. Once the vector information is forwarded to the processor).

As for claims 3, 23 and 41, Jayakumar teaches an interrupt staging unit for storing value representative of the interrupt request of highest priority (see figure 2, IRR 218, ISR 220 and column 6 lines 17-25);

an interrupt transmission unit for transmitting a notification signal to the microprocessor indicating that a new interrupt request is stored in the interrupt storage means (see figure 2, IRR 218, ISR 220 and column 6 lines 17-25).

As for claim 4, Jayakumar teaches interrupt staging unit is an interrupt vector register (see figure 1, interrupt vector register 124).

As for claim 5, Jayakumar teaches IRQ signal (see figure 1, interrupts 110).

As for claim 6, Jayakumar teaches an interrupt notification signal reception unit (see figure 1, acceptance logic unit 112);

interrupt access unit for reading the value representative of the new interrupt request stored within the interrupt staging unit (see figure 1, interrupt vector register 124 and column 5 lines 22-26).

a context storage unit for saving a current context of the microprocessor (see figure 2, IRR 218, ISR 220 and column 6 lines 17-37);

an interrupt stack controller for determining whether a current interrupt service routine is being executed, and if so, for storing the interrupt request associated therewith in an interrupt stack (see figure 2, IRR 218, ISR 220 and column 6 lines 17-37);

an interrupt service routine execution unit for executing an interrupt service routine associate with the new interrupt request value read from the interrupt staging unit (see figure 2, IRR 218, ISR 220 and column 6 lines 17-37).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 15-18, 32-36 and 48-51 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Jayakumar.

As for claims 15-18, 32-36 and 48-51 Jayakumar teaches interrupt prioritization unit determines a relative priority of interrupt requests from among a plurality of priority levels (see figure 1, interrupts 110, prioritizer 118 and column 4 lines 63-66).

Jayakumar does not expressly teach round robin method for priority interrupt level. However, Jayakumar teaches handling interrupts are instructed by prescribed set of rules. Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to prescribed set of rules into round robin method because the round robin is known for fairness priority scheme that guaranteed any request agents ownership after a request is made.

3. Claims 19, 37 and 52 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Jayakumar in view of Benzel et al. 5,421,027 referred hereinafter "Benzel".

As for claim 19, 37, 52 Jayakumar does not expressly teach power control to awaken computer system. However, Benzel teaches power control to awaken computer system after receiving wake up interrupt (column 4 lines 9-13 of Benzel). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to combine the teaching of Benzel into the teaching of Jayakumar because Benzel providing power control to conserve power (see column 1 lines 30-38 of Benzel).

4. Claims 20, 38 and 53 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Jayakumar in view of Muller, Mike (1993) ARM6 a high performance low power consumption macrocell. IEEE pgs. 80-87 referred hereinafter "Muller".

Claims 20, 38 and 53 Jayakumar does not expressly teach distinguishing between IRQ and FIQ interrupt request. However, Muller teaches identifying interrupt request (see pages 80-87 of Muller). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to combine the teaching of Muller into the teaching of Jayakumar because Muller distinguished different type of interrupts when an interrupt occurs thereby providing smooth operation and increases system performance because the system would response correspondingly to the interrupt.

Examiner's Statement of Reasons for Allowance

5. Claims 7-14, 24-31 and 42-47 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is an Examiner's statement of reasons for the indication of allowable subject matter: Claims 7-14, 24-31 and 42-47 are allowable over the prior art of record because the Examiner found neither prior art cited in its entirety, nor based on the prior art, found any motivation to combine any of the said prior arts. Prior art fails to teach or fairly suggest wherein the interrupt service routine execution unit also detects completion of the interrupt service routine, determines whether the interrupt staging unit contains another value representative of an interrupt request and, if so, executes an interrupt service routine associated with the interrupt request value read from the interrupt staging unit and, if not, retrieves an interrupt request, if any, stored at the top of the interrupt stack and the context saved in the context storage unit and resumes execution based upon that context.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tim T. Vo whose telephone number is 703-308-5862. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-2100.

Tim T. Vo
Examiner
Art Unit 2189

T.V
11/25/03